

TG12864-COG7



Graphic Type

Feature :

- 1、128x64 dot-matrix
- 2, STN/Transmissive/Positive/Y-G
- 3、Non-Backlight
- 4. Operating Temp.: $-10^{\circ}C \sim +60^{\circ}C$
- 5、1/65 duty cycle, 1/9 Bias
- 6、Built-in Controller(NT7538H or equivalent)
- 7、Viewing angle: 6 o'clock

Absolute Maximum Rating:

Item	Symbol	Standard value			Unit
		$\mathbf{M}_{\mathbf{IN}}$	T _{YP}	M _{AX}	Unit
Power supply for logic	V_{DD} - V_{SS}	-0.3		+4.0	v
Input voltage	VI	-0.3		V _{DD} +0.3	V

Electrical Characteristic: $(VSS=0V, Ta = 25^{\circ}C)$

Parameter	Symbol	Condition	M _{IN}	T _{YP}	M _{AX}	Unit
Supply voltage for logic	V _{DD}		2.8	3.0	3.2	v
Supply current for logic	I _{DD}			1		mA
Operating voltage for LCD	V _{LCD}	+10°C				V
		+25°C		9.0		V
		+60°C				V
Supply voltage for Backlight	V _{BL}					v
Supply current for Backlight	\mathbf{I}_{BL}					mA

Interface Pin Connections:

Pin No.	Symbol	Level	Description
1~2	NC		Non-connection.
3	/CS1	H/L	/CS1="L", Chip select becomes active.
4	/RES	H/L	When /RES= "L", the settings are initialized.
5	A0	H/L	$A0 = "H": D0 \sim D7$ are display data $A0 = "L": D0 \sim D7$ are control data
6	/WR	H/L	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. R/W = "H": Read R/W = "L": Write
7	/RD	H/L	When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080MPU, and the NT7538 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.

Interface Pin Connections :

Pin No.	Symbol	Level	Description	
8~15	D0~D7	Н/L	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7 serves as the serial clock input terminal (SI) and D6 serves as the serial clock input terminal (SCL). When the serial interface is selected, fix D0-D5 pads to VDD or VSS level. When the chip select is inactive, D0 to D7 are set to high impedance.	
16	VDD	+3.0V	Supply voltage for logic operating.	
17	VSS	0V	Ground.	
18	VOUT		DC/DC voltage converter output.	
19	CAP3+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	
20	CAP1-		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	
21	CAP1+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	
22	CAP2+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	
23	CAP2-		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	
24	NC		Non-connection.	
25	V1		LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver	
26	V2		or an operation amplifier for application. Voltages should be according to the following relationship: $V0 \ge V1 \ge V2$	
27	V3		≥V3≥V4≥VSS2. When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is	
28	V4		bit	
29	V0		16 bits 56/00 46/00 26/00 16/00 17 bits 67/00 27/00 17/00 18 bits 75/00 56/00 26/00 17 bits 66/00 26/00 16/00 18 bits 75/00 56/00 16/00 16 bits 66/00 26/00 16/00	
30	VR		Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.	
31	NC		Non-connection.	
32	C86	H/L	C86 = "H": 6800 Series MPU interface C86 = "L": 8080 Series MPU interface	
33	P/S	H/L	This is the parallel data input/serial data input switch terminal $P/S = "H"$: Parallel data input $P/S = "L"$: Serial data input The following applies depending on the P/S status: $\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$	
34	NC		Non-connection.	
35	IRS	H/L	This terminal selects the resistors for the V0 voltage level adjustment. IRS = "H", Use the internal resistors IRS = "L", Do not use the internal resistors The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pad is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.	
36	NC		Non-connection.	

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